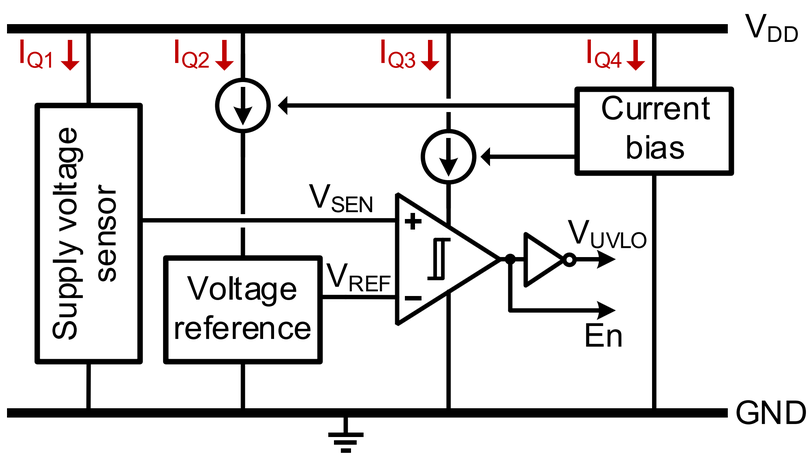
IDEC Chip Design Contest

A 10.9-nA Self-Biased Standalone Under-Voltage Lockout Circuit for Always-On Power Monitoring at 5 V

Energy-Efficient Circuits and Systems Lab

Seongmin Bae, Mina Shin, Kunhee Cho
Sungkyunkwan University, Suwon, Korea
SK Keyfoundry, South Korea

Motivation



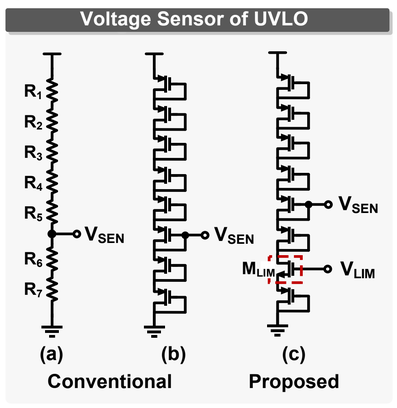
❖ Limitation of Conventional UVLO

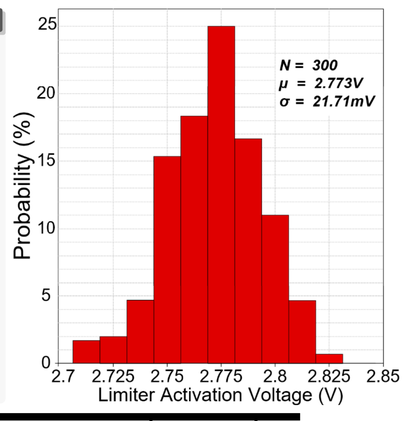
- ✓ Continuous static current from the resistive divider and bias circuits
- ✓ Difficulty in achieving nanoampere-level IQ for always-on operation
- ✓ I_Q increases with V_{DD}, degrading standby efficiency

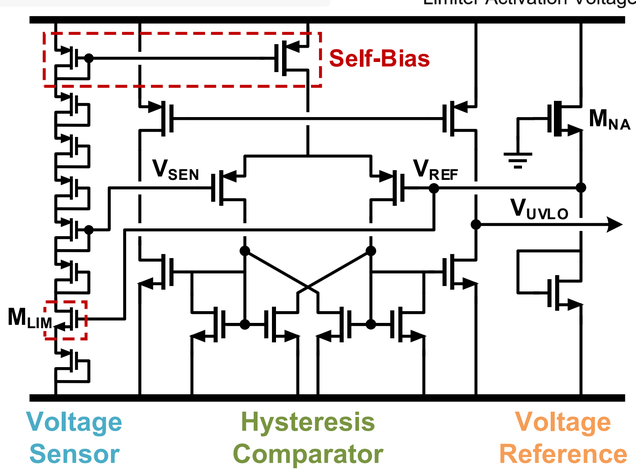
❖ Key Advantages of the Proposed UVLO

- ✓ Self-biased architecture eliminates extra bias circuits
- ✓ MOS-diode divider with current limiter suppresses I_Q increase
- ✓ Achieves **10.9 nA** I_Q at 5 V with **862× current reduction**

Operation







❖ Sensing Voltage V_{SEN}

$$V_{SEN} \approx \frac{2}{7} V_{DD}$$

❖ Current limiter turns on when

$$V_{SEN} > V_{LIM} + \Delta$$

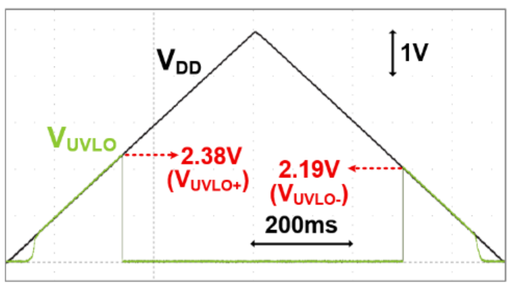
$$\Delta = V_{SG,M6} - V_{TH,MLIM}$$

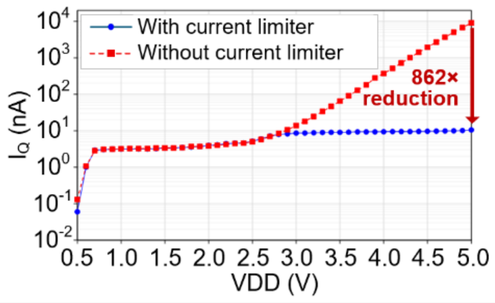
❖ A subthreshold PMOS current mirror provides self-biases for the comparator, eliminating extra bias circuitry

❖ A native-FET-based VREF provides a compact low-current reference

$$V_{REF} \approx 0.65\,V$$

Measurement Results





Parameter	This work	APEC' 17	JSSC' 23	Integration' 23	TI TPS7A02
Process	180 nm CMOS	1.2 μm BCD	500 nm BCD	250 nm BCD	N/A
Quiescent Current @ V_{DD}	**10.9 nA** @ 5 V	27 μA @ 15 V	583 nA @ 12 V	5 μA @ 3.3 V	25 nA @ 5 V
V_{UVLO+} / V_{UVLO-}	2.38 V / 2.19 V	1.3 V / 1.12 V	N/A	2.37 V / 1.93 V	8.72 V / 8.24 V
Hysteresis	0.19 V	0.48 V	-	0.44 V	0.18 V
Area	0.014 mm²	N/A	0.168 mm²	0.226 mm²	N/A

❖ Implemented in **180 nm Process**

❖ Achieves ultra-low quiescent current of **10.9 nA** at 5 V

❖ Maintains nearly constant current across a wide VDD range due to the voltage limiter

❖ Demonstrates up to **862×** reduction in current compared to conventional structures

References

[1] K. Song, *APEC*, Mar. 2017, pp. 1085–1089
[2] Y. Wen, *JSSC*, Feb. 2023, pp. 497–507
[3] X. Liu, *JSSC*, Jul. 2024, pp. 2272–2285
[4] Texas Instruments, TPS7A02, Datasheet

Acknowledgement

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